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Performance Analysis of LDPC Decoding Techniques

Abdel Halim A. Zikry, Ashraf Y. Hassan, Wageeda I. Shaban, Sahar F. Abdel-Momen.

Abstract: Low density parity checking codes (LDPC) are one of the most important issues in coding theory at present. LDPC-code are a type of linear-block LDPC-codes. Channel coding might be considered as the finest conversant and most potent components of cellular communications systems, that was employed for transmitting errors corrections imposed by noise, fading and interfering. LDPC-codes are advanced coding gain, i.e., new area in coding. the performances of LDPC-code are similar to the Shannon-limiting, this led to the usage of decoding in several applications in digital communications systems, like DVB-S2 and WLAN802.1.. This paper aims to know what is LDPC, what its application and introduce encoding algorithms that gives rise to a linear encoding time and also show that the regular and irregular LDPC performance and also introduce different methods for decoding LDPC. I discuss in detail LDPC decoding algorithm: bit flipping algorithm, as a type from hard decision .belief propagation algorithm, sum product algorithm and minimum sum algorithm as examples from soft decision .I expect that at least some students or researchers involved in researching LDPC codes would find this paper helpful.

Keywords: Low Density Parity Check Code LDPC, Parity Check Matrix H.

I. INTRODUCTION

T his is One of the newest subjects in coding theory today is low density parity-check codes. a class of linear block LDPC codes is the Low-density parity-check (LDPC) codes. Channel coding can be seen as the best known and most effective component of cellular communication systems used to correct noise, interference and fading transmission errors. Low-Density Parity-Check (LDPC) codes are a greater gain in coding, i.e. a new coding area. The performance of LDPC code is restricted to the Shannon limit, making decoding very for many digital communication desirable systems applications, such as DVB-S2 and WLAN802.11.in this paper we are intended to attempt to discuss the following, such as What are LDPC codes? So why do we take an interest in them? and H0w, are they functioning? Humanity has been engaged in discovering and understanding the World since the dawn of time. The need for higher-speed wireless communication is likely to continue for the near future .The channel settings can suffer as interference, noise and fading as a message transfer. from the transmitter to the receiver.

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This creates signal errors that make its recovery at the receiver almost unlikely. Interference, multi-path, and time variation are inherent features of wireless channels that make it difficult to reach, differences between LDPC codes and other codes: The big difference is the sparseness of the parity check matrix, Besides the sparseness, the other difference between LDPC codes and classic block codes is the encoding technique. Classic block codes are generally decoded with Maximum likelihood (ML) decoding algorithms however are generally short and algebraically designed to reduce complexity. LDPC codes are decoded iteratively using a graphical representation of their parity-check matrix, so they are designed with the properties of H as a focus.[4] high data rates on these channels. This problem becomes even more challenging if we Considering the practical need for implementation of low-complexity and low-power systems, the need to find effective solutions to the above problem has generated a great deal of research on wireless communication systems in recent years. Low-density parity-check (LDPC) codes can closely approach the Shannon limit capacity in channel coding theory and become one of the most promising channel codes in the world of error control coding. The reliability of error-correcting codes (ECCs) that approach the Shannon limit. Several approaches have been developed to assist the receiver recover the original signal. There really are two types of techniques for correcting errors, ARQ (Automatic Repeat Request) and FEC (Forward Correction of Error). In ARQ, re-sending is a request when the receiver discovers an error in the received information. In several cases, it is not possible to re-send data, FEC If redundant bits are added to the data, these redundant bits really had no new information, but are later used to identify and correct the error according to redundant bits called parity bits [1]. In the irregular structure of the LDPC, the framework gives rise to ensembles that are not possible. In LDPC designs, various new characteristics can be introduced and new constraints brought to bear. This framework has already been used to generate LDPC codes that perform better than traditional irregular LDPC codes over standard channels such as the AWGN channel, particularly for short block lengths, while necessitating lower complexity. It was used to adapt an LDPC design to the structure of a turbo equaliser receiver, achieving significant gains[2]. The framework produces very low high performance codes and high rate codes with low error floors. [3]





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II. CONTEXT DETAILS

We are just going to focus exclusively on binary linear codes. The binary linear code C of block length n is a vector space F_2^n where $F_2 = \{0, 1\}$ is the field with two elements. The rate of C, denoted by R(C), equals to $\frac{k}{n}$ where k is the dimension of C (as a vector space over F_2); such a code is also referred to as an [n, k] code. Being a linear subspace of dimension k, the code C can be described as the core of a matrix $H \in F_2^{(n-k) \times n}$, so that $C = \{H\}$, where c = 0(codewords ^c are considered column vectors for this description). The matrix H is called the parity check matrix of the code C. In general, any choice of H whose rows form a basis of the dual space $C \Vdash \{x_c^t = 0\}, \forall c \in C$. Well, that describes the same code. Of particular interest to us here are codes that recognize a sparse parity check matrix. In particular, we will study the Low-Density Parity Check (LDPC) have been used.introduced and studied in Gallagher's Excellent work [5]. M bits N-M bits





A. Definition of parity Check code.

LDPC codes are described by a parity check matrix all of whose rows and columns have at most a fixed constant number of 1's (the constant is independent of n). A convenient way to describe an LDPC code is in terms of its factor graph. This is a natural bipartite graph defined as follows. On the left side are n vertices, called variable nodes, one for each codeword position. On the right are m = n - k vertices, called check nodes, one for each parity check (row of the parity check matrix). A test node is adjacent to the corresponding codeword symbols of all variable nodes in this parity check. The parity control matrix of the code, in other words, is exactly the bipartite adjacency matrix of the factor graph. Regular LDPC codes are a special class of LDPC codes, and the factor graph is both left-regular and right-regular. The model originally studied by Gallagher[6], and also in the works of Mackay and Neal[7, 8] and Sipser and Spielman, were in fact the regular LDPC codes that ignited the revival of interest in LDPC codes after more than 30 years given that Gallagher's LDPC codes, based on non-regular graphs, called irregular LDPC codes, came to popularity beginning in the work of Luby et al [9, 10] (One of the major conceptual strides made in these works was exploring codes based on irregular graphs). Later in the article, we will return to this aspect. (3,6)-regular LDPC codes where variable nodes have degree 3 and test nodes have degree 6 are the typical choice of regular LDPC codes (with a rate of 1/2) [11].

III. CHANNEL CODING

In the wireless communication system, because of channel noise, the signal bearing information produced by the transmitter can not be interpreted correctly by the receiver. The design of a good communication system would decrease the possibility of error in the received signal by allowing the transmitting capacity and usable channel bandwidth to be optimally exploited, while retaining sufficient system complexity. Fig. 2 is a block diagram with various functional representations[12].



Fig. 2 show that blocks in the communication system [13].



Fig. 3 is a block diagram with various functional representations[14].

IV. SHANNON'S CHANNEL CAPACITY THEOREM



Fig. 4 show that LDPC code close to Shannon limit[15].

One of the foremost important people that made great contributions to modern communications, Shannon, an American mathematician put ahead channel capacity in 1948., he figured out that Channel capacity refers to the maximum transmission rate for a particular channel, which means that for every bit error rate, efficient communication can be achieved when the transmission rate is equal to or lower than this maximum rate. On the other hand regardless what kind of transceivers are used the efficiency of transmission can not be assured at a higher transmission rate. This concept is often referred to as the Shannon theorem. [13]. The Shannon channel coding theorem in information theory is known to have encouraged the improvement of error control codes. It states that all the data rates R_b less than the channel capacity *C* can be achieved with an arbitrarily small probability of error P_e , where C is given by the Shannon-Hartley formula.[14].



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$$C = W \times \log_2 \left(1 + \frac{P}{N_0 W} \right)$$

$$\frac{C}{W} = \left(1 + \frac{E_b}{N_0} \frac{R_s}{W} \right) bits$$
(1)

where,

С = channel capacity, bits/sec, W =transmission bandwidth, hertz, $P = E_b R_s = \text{signal}$ power, watts, $N_0 =$ single-sided noise power spectral density, watts/hertz,

 E_b = energy per bit of the received signal, joules, and R_s = source data rate, bits/sec.[15]

V. PRELIMINARIES

Coding: The transfer of data to another type for some reason. **Source Coding:** The goal is to reduce the redundancy of data in the.

Channel Coding: The goal is to overcome channel noise bits in the bit stream of the sender to create a codeword..

Encoder and Decoder:

The encoder adds that the redundant bits are used by the decoder to detect and/or correct as many bit errors as the basic error control code allows.

Modulator and Demodulator: The modulator converts the digital output of the encoder into a channel-specific format that is normally analogue (e.g., a telephone channel). In the presence of noise, the demodulator tries to retrieve the correct channel symbol. The decoder tries to correct any errors that occur when the wrong symbol is chosen.

Bit-Error-Rate (BER):

The probability of an error in bits. For an error management code, this is always the figure of merit. We want to keep this number small, less than 10⁻⁴ usually. The bit-error rate is a useful measure of system quality on an independent error channel, but on bursty or dependent error channels, it has little meaning. **Burst Errors:** Errors that are not independent. For example, channels with deep fades experience errors that occur in bursts. Because the fades make consecutive bits more likely to be in error, the errors are usually considered dependent rather than independent. In contrast to independent-error channels, burst-error channels have memory.[16]

VI. HISTORY OF LOW-DENSITY PARITY CHECK CODES

In 1948, Shannon published his famous paper on the capacity of channels with noise. In 1963, Robert Gallagher wrote his Ph.D. dissertation "Low Density Parity Check Codes". He introduced LDPC codes, analyzed them, and gave some decoding algorithms Because computers at that time were not very powerful, he could not verify that his codes could approach capacity. In 1982, Michael Tanner considered Gallagher's LDPC codes, and his own structured codes. He introduced the notion of using bipartite graph, sometimes called a Tanner graph. In 1993, Turbo Codes were introduced. They exceeded the performance of all known codes, and had low decoding complexity. In 1995, interest was renewed in Gallagher's LDPC codes, led by David MacKay and many others. It was shown that LDPC codes can essentially achieve Shannon Capacity on AWGN and Binary Erasure Channels [17].

i. Form of the System

The LDPC system model consists of transmitter, AWGN channel and a receiver



Fig. 5 Form of the system[16].

ii .Transmitter of LDPC system

The transmitter of the LDPC system consists of creating LDPC matrix, eliminating length-4 cycle, generating parity check matrix using LU factorization on LDPC matrix. The generated data is then encoded using the parity check matrix. BPSK technique is used for modulation.[18]

AWGN Channel



.Fig. 6show that AWGN additive white Gaussian noise channel[19].

High data rate communication over additive white Gaussian noise channel (AWGN) is limited by noise. The received signal in the interval $0 \le t \le T$ may be expressed as r(t) = (t) + n(t), where n(t) denotes the sample function of AWGN process with power (spectral density)[19].

VII. LITERATURE SURVEY

Significant research the reliability of the systems was once begun for a long time ago. In the preceding work, researchers tried to decrease the design complexity, power consumption and increase the speed of LDPC decoder.In2020, by publishing a paper entitled Joint optimization of interleaving and LDPC decoding for burst errors in PON systems, Lei Zhang et al. improved decoding performance by explaining that the proposed scheme is more characteristic at greater lengths of burst-error. With a burst-error length of 1500 and a pre-BER of 0.0243, the post-BER values of 8×2400 block interleaves, random interleaves and convolutionary interleaves are 9.5117×10⁻⁵,2.4372×10-5 and 1.9461×10⁻⁵, respectively. On the other hand, our proposed scheme has two orders of post-BER magnitude with better performance $(1,5672 \times 10^{-7})$. The simulation results therefore justify our design rule, which achieves a common optimization of interleaving. and LDPC decoding, which can significantly improve the performance of decoding in PON systems that deploy LDPC codes.[20]. Hossein Gharaee and et al presented "A High-throughput FPGA Implementation of

Quasi-Cyclic LDPC Decoder" in their work in 2017. In their papers, an FPGA implementation of a partial-parallel QC-LDPC

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decoder was proposed based on the sum-product algorithm. This is a modified version of the TPMP1 algorithm to increase the number of clock cycles, cost efficiency and power consumption. The results indicate that by implementing the sum product algorithm in the proposed time schedule, this decoder showed maximum throughput with lower power consumption and area.[24]

As of 2018. Ahmed Abdel-Mouleh, introducing thesis is titled "Non-binary LDPC codes associated with high-order modulations," which he devoted to exploring the relationship of non-binary LDPC codes (NB-LDPC), with high-order modulations. And aims to increase the spectral performance of future wireless communication systems. Their approach seeks to take full advantage of the direct correlation between NB-LDPC codes with modulation constellations of the same cardinality over a Galois field. The second contribution concerns a new method for designing an advanced CM communication scheme for high-spectral efficiency. Mutual optimization of the NB-LDPCcode and M-QAM modulation, the benefit of using the same order for both (q=M), is the key concept behind the technical method. This approach is different from what is subsequently achieved, where the codes and modulation of the NB-LDPC are optimised in a disjointed way[26].In 2018, a novel was proposed by Albashir Adel Youssef and others in which comprehensive performance evaluations of different LDPC decoding algorithms are used to enhance communication and decrease the complexity of implants for WBAN channel implants. In the BER, prominence has been shown by the proposed low-complex LDPC hybrid decoding algorithm, decoding iterations, hardware complexity, number of operations, decoder convergence, decoder throughput, statistical properties and decoding time. Because of the use of the lowest number of iterations necessary, hardware complexity, decoder convergence, decoder throughput, the proposed algorithm achieved the lowest level of complexity, Besides that, the In particular, modest LDPC matrices and Bottommost E b = N 0S were occupied with the minimum number of operations. In comparison, the proposed algorithm, similar to MIERRWBF and BMIERRWBF, achieved a lower decoding time, performed a progressive number of decoding operations and obtained the highest resulting efficiency among all algorithms developed. Furthermore, relative to other algorithms, the proposed algorithm achieved the fastest convergence and conducted a non-parallel statistical analysis while retaining the same statistical analysis. Preserving comparable decoding parameters[27].

VIII. WHY LDPC CODES RAISE OUR ATTENTIONS?

How they are decoded is the main difference between classical block codes and LDPC codes. Classical block codes, such as decoding algorithms, are generally decoded with ML and are therefore generally short and algebraically constructed to make this role less complex. However, using a graphical representation of their parity-check matrix, LDPC codes are iteratively decoded and are therefore designed with the properties of H as a priority and appear to have better block error performance and better performance performance on bursty channels. They are more suited for high rates and can really be designed for roughly any block rate and length. (The rate of turbo codes is typically modified by way of a puncturing method that needs an additional design step in comparison.), Their error level tends to occur at a lower rate. Interleaves may not be needed for the encoder and decoder. For channel collection, a single LDPC code may be universally sufficient. There are iterative LDPC decoding algorithms that are simple to implement, have moderate complexity (which scales linearly with the block length), and are parallel to hardware. In particular, LDPC decoding seems to be less complex than turbo decoding using the BCJR algorithm using the Credential Propagation (Sum Product) algorithm. Inherently, LDPC decoders check if a codeword satisfying the check equations has been found and otherwise announce a decoding failure (on the other hand, turbo decoders typically need to perform additional operations to calculate a stop criterion, and even then it is not clear if the result of decoding corresponds to a codeword satisfying the check equations). [28]. The LDPC code decoding method is an iterative process with low computational complexity based on a sparse matrix, while the parallel structure provides a chance to implement hardware. Since it is simple to create the LDPC code rate, system optimization with a versatile and self-adapted coding system is possible. When it comes to high-speed data transfer or high-performance applications, LDPC performs better compared with Turbo LDPC codes. Another benefit of LDPC is low error flooring, which enables low-bit error. rate (BER) applications to operate, such as wire communication, deep space communication and storage media, [29].

iii . LDPC APPLICATIONS

Today, because of its superior decoding performance as benefits with well as the associated hardware implementations, such as low-cost high-throughput capabilities and power efficiency, LDPC codes have achieved widespread applications in modern communication systems. As a consequence, other well-known FEC systems are increasingly being replaced by LDPC codes. Several recent communication standards have been introduced, such as 802.11n (Wi-Fi), 802.11ad (WiGig, 802.16e (WiMAX), 802.15.3c (WPAN) and seconds, for example. Irregular LDPC codes are used in the high definition satellite television (HDTV) standard, which is known as the Digital Video Broadcasting (DVB-S2) transmission system standard. From optical networks to digital storage, DVB-S2 is considered for a wide range of applications. LDPC codes have also been proposed as a possible candidate for a 5 G cellular system[11]. The LDPC code has a wide range of applications, such as satellite communications (DVB-S2), storage devices, optical communications, Wi-Fi and WiMAX mobile[22], and is selected as the channel code type for the mobile 5 G data channel transmission system[23]

iv . LDPC IMPROVEMENT CODES

one of the forward error correction codes that Robert Gallagher invented in 1960 is LDPC. Since the difficulty of

implementing hardware at that time was overlooked until MacKay and Neal rediscovered it in 1996.[34] It was considered a

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code for capacity-approaching. The phrase low-density comes from the matrix of parity check, in which the number of zeroes, also called Gallagher codes, is much smaller than the number of zeroes. This concerns one of the kinds of block codes in which there are K information bits encoded and decoded by themselves in a message separated into two blocks[33]. There are two matrices in the LDPC code, the generator matrix (G-matrix) on the encoder and the parity matrix (H-matrix) on the encoder.

v. LDPC CODES TYPES



.Fig. 7 show that types of LDPC codes.

If w_c is constant for every column, w_r is constant for every row and w_r is constant for every row, the LDPC code is said to be regular. It is called irregular an LDPC which is not regular.

Example.1.

A regular parity-check matrix for the code in with $w_c = 2$, $w_r = 3$, which satisfies is

$$\mathbf{H} = \begin{pmatrix} 1 & 1 & 0 & 1 & 0 & 0 \\ 0 & 1 & 1 & 0 & 1 & 0 \\ 1 & 0 & 0 & 0 & 1 & 1 \\ 0 & 0 & 1 & 1 & 0 & 1 \end{pmatrix}$$

Definition LDPC Codes

An LDPC code is a linear block code defined by a (M, N) sparse parity-check matrix denoted by H. consider a linear (N, K) block code C, which H has N rows r_n , where n = 0, ..., N - 1 and M = N - K linearly independent columns h_m , where m = 0, ..., N - K - 1. As their name suggests, sparse or low-density means that the paritycheck matrix contains only few 1s in comparison to the amount of 0s. This sparseness of H is

essential for iterative decoding complexity, which only increases linearly with the length of the code[7]. The other type is the irregular LDPC code which do not have uniform row and column weights. Irregular LDPC codes are the one in which **H** The density is poor, but there is no constant number of 1s in any row or column.

Example .2. of irregular LDPC code

/0	0	0	1	0	0	1	1 1 0 0
1	0	0	0	0	1	0	1
0	1	1	0	1	0	1	0
/0	1	1	0	1	0	1	0/

Matrix shown that irregular LDPCcode

IX. REPRESENTATION OF THE LDPC CODE

No analytical (algebraic or geometric) approach has been used to design such codes, while LDPC codes have been shown to achieve excellent efficiency. Only one class of pseudo-random LDPC codes was given by Gallagher . Strong LDPC codes, particularly long codes, that have been found are largely computer-generated. Due to the absence of code structure, such as cyclic or quasi-cyclic, the encoding of these large computers generated by LDPC codes is very complex. structure. In addition, their minimum distances are either poor or difficult to determine[17]. There, essentially, are two different possibilities to represent LDPC codes. Like all linear block codes, they can To be identified by matrices. A graphical representation is the second possibility. These two representations are completely identical, and based on the types of simplification it brings to solve the problem, we choose one or the other.

A 1 .Matrix Representation

/1	1	0	0	1	1	0)	
1	0	0	1	0	1	1)	
\backslash_1	0	1	0	1	0	$\begin{pmatrix} 0\\1\\1 \end{pmatrix}$	

Each column represents a coded bit in the check matrix H, while each row equates to a check sum. The number of non-zero elements for each column is known as column weight (w_c), and the number of non-zero elements for each row (w_r) is also referred to as row weight. The matrix of its size M-N) with M = N-K. More precisely, in the form of a linear system, the parity check matrix defines the relation between the code word symbols, i.e. Hx=0, 0. Gallager claimed that this matrix ought to have a limited number of non-LDPC codes when implementing LDPC codes. There are zero elements. A small proportion of symbols would provide the low density matrix of each interaction. In the case of a hierarchical code, the symbol corresponds to every column, The first column K corresponds to symbols of information, and the last column N K corresponds to symbols of redundancy. The LDPC code with N=1/4 8 and K=1/4 4 is defined by the parity matrix, for example [27].

A 2. Graphical Representation

The second representation of the LDPC codes is a bipartite graph, also referred to as the Tanner graph. The graph is bipartite if there are two sets of vertical nodes U and V and a set of edges such that each edge connects the node U with the node V. You can describe the LDPC code from a Tanner graph whose node set V (variable nodes) represents the codeword symbols and all the correct nodes, denoted (consensus nodes).. The symbol sequence would then be a valid code word if and only if the number of symbols corresponding to the vector nodes for each node limit is zero. The Tanner graph with the code for the LDPC is [29].



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Fig. 8 shown that Tanner graph

Tanner considered LDPC codes and showed how the so-called bipartite graph, also known as the Tanner graph, could be effectively represented, providing a complete representation of the code and helping to understand the decoding algorithm[28].

Encoding

Usually, LDPC codes are constructed by creating a sparse check matrix H first and then evaluating the corresponding generator matrix G. The complexity of encoding through the standard relationship c = Gu in block length N is not sparse, but there are different types of LDPC codes which have a deterministic structure that reduces the complexity of encoding.based on finite geometries that lead to cyclic or quasi-cyclic LDPC codes that can be encoded using Shift registry circuits, such as some LDPC code designs, and a deterministic str, on the other hand, allows efficient encoding[32].

X. CONSTRUCTION METHODS FOR LDPC CODE

Based on construction methods, the LDPC codes can also be divided into two other classifications. In the absence of a deterministic structure, the encoding complexity can still be significantly decreased by an encoding process based not on the matrix of the G generator but directly on the matrix of the H check.

B 1. Gallagher's LDPC code construction

The technique proposed the following random construction of a regular LDPCcode parameters are chosen such that $N = p\omega_{c}$ and $M = p\omega_{r}$ withan integer factor p, so that $N/\omega_{c} = M/\omega_{r} = p$. The density of H follows from $\rho = \omega_{r}/M = 1/p$. Thus, the code is an LDPC code if p. It is picked to be big enough. Then, the $N \times M$ check matrix H is constructed as a block-rowmatrix composed of $\omega_{r} \geq 3$ blocks H_{i} , where $i = 1, ..., \omega_{r}$ of dimension $N \times p$ each, i.e., $(H_{1}, ..., H_{\omega_{r}})$

Example

Given the regular (Gallagher) LDPC code parameters $N = 20, k = 5, \omega_r = 4$ and $\omega_c = 3$, the resultant ^H is given by the following ^H matrix

H =			

1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	1	0	0	0	0	0	0	1	0	0	0
0	0	1	0	0	0	1	0	0	0	0	0	0	1	0	0	0	1	0	0
0	0	0	1	0	0	0	0	0	0	1	0	0	0	1	0	0	0	1	0
0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1
1	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0
0	1	0	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	1	0	0	0
0	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0	0	1

Mostly for large block lengths, the ability of LDPC codes to perform near the Shannon limit of a channel exists.. For example, Simulations have been carried out throughout the system. $0.0045 \ dB$ of the Shannon limit at a biterror rate of 10^{-6} with a block length of 10^{7} .[25].

B 2.Mac-Kay's Construction Technique

	1	0	0	0	0	1	0	1	0	1	0	0]	
	1	0	0	1	1	0	0	0	0	0	1	0	
	0	1	0	0	1	0	1	0	1	0	0	0	
	0	0	1	0	0	1	0	0	0	0	1	1	
H =	0										0		
	0	1	0	0	1	0	0	0	1	0	1	0	
	1	0	0	1	0	0	1	0	0	1	0	0	
	0	1	0	0	0	1	0	1	0	1	0	0	
	0	0	1				0					1	

Suggests that the encoding should be performed by using the generator matrix G obtained through Gaussian elimination from H. This approach is not efficient because even though the Parity-Check matrix is sparse, the generator matrix is not generally effective. The encoding complexity of the long block length codes generated in this way will therefore be high.[26] In this approach, columns in H are generated from left to right until the whole check matrix is created. Column weight can be ensured to meet the demand as a premise and the location of non-zero elements is selected randomly between rows as long as the overall allocated row weight is not exceeded. reset of H or cancelation and reset of some rows from right to left in the matrix occurs when the row weight cannot meet requirements when setting the last column.[27]

B 3 .Cyclic Shift Matrices-based algebraic construction A basic algebraic structure of the check matrix H with a

column weight ω_c and row weight is ω_r as follows for an arbitrary $p \ge (\omega_c - 1)(\omega_r - 1) + 1$ and an arbitrary $J \in \{0, \dots, p-1\}$, consider $p \times p$ cyclic shift matrix I_J that is obtained by cyclically shifting each column of the $p \times p$ identity matrix I down by J positions, for example, for



$$h = \begin{pmatrix} 0 & 0 & 0 & \cdots & 0 & 1 \\ 1 & 0 & 0 & \cdots & 0 & 0 \\ 0 & 1 & 0 & \cdots & 0 & 0 \\ 0 & 0 & 1 & \cdots & 0 & 0 \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ 0 & 0 & 0 & \cdots & 1 & 0 \end{pmatrix}$$

Note that $J_1 = J_1^{J}$ then, the check matrix constructed as

	/ I	Ι	Ι		$I \setminus$
	Ι	\boldsymbol{J}_2	$oldsymbol{J}_4$		$oldsymbol{J}_{2(\omega r-1)}$
H =	Ι	J_3	$oldsymbol{J}_{\mathfrak{6}}$		$J_{3(\omega r-1)}$
	1		:	1	:
	I	$oldsymbol{J}_{\omega^{c-1}}$	$oldsymbol{J}_{2(\omega c-1)}$		$J_{\scriptscriptstyle (\omega c-1)(\omega r-1)}/$

XI. DECODING METHODS

The near-capacity performance of low-density parity-check codes was first demonstrated with efficient decoding algorithms like min-sum (MS) and sum-product (SP). These two decoding algorithms take advantage of the sparseness of the parity-check matrices of LDPC codes, since the complexity of the MS and SP algorithms scales in proportion to the number of binary 1s in the parity-check matrix. However, due to the sub-optimality of the MS and SP decoders, new decoding algorithms for LDPC codes have been created along with variations of the SP and MS decoders in an attempt to improve their performance.[19].With more or less the same iterative decoding algorithm, distinct authors come up separately. They call it various names: the algorithm of the sum-product, the algorithm of the propagation of beliefs, and the algorithm of message passing. This algorithm has two derivations: hard-decision and soft-decision schemes.[15] Several decoding approaches have been suggested based on iterative decoding, including high-parallel and low-parallel degrees. For high-parallel decoders, check node 1 units, variable node units and interconnects are integrated in a single chip. Both messages are measured in parallel and each decoding operation is done in one clock cycle.there is a short decoding delay and quick throughput for decoders with high parallelism, but they have a large silicon region. Low-parallel decoders, on the other hand, need fewer processing units and higher-density memories instead of separate registers, so the area is smaller and it provides lower throughput[14].

XII. BASICS OF ITERATIVE DECODING

In order to converge towards a global solution, the idea behind iterative principles is to solve a global problem by splitting it into smaller problems that are easier to solve and iterate between them. The basic building blocks and principles of iterative decoding systems that will be used in this thesis are introduced in this section. We present, first of all the channel models and their unified definition. Instead, part codes and the definition of concatenated codes was applied to establish successful codes.codes that are iterative algorithms that can be decoded. Finally, turbo codes and low-density parity-check (LDPC) codes, the most popular iterative decoding codes, are described.[14].

I. Hard Decision Decoding

- Simple decoder construction.
- Input values are not considering the channel nformation.
- Bit flipping algorithms.
- Faster convergence with significant impact on error correcting characteristics

II. Soft Decision Decoding

- Complicated decoder construction
- · Channel information is considered in decoding process
- Message passing algorithms Slow converging, but more powerful methods of decoding.[16].





Fig. 9 show that bit _flipping

For every bit received, Bit Flipping is based on a hard start decision[28]. The hard binary decision is taken by the detector on each obtained bit and transferred to another decoder. The message is passed from the nodes of the code tanner graph during bit flipping. Each Bit Node sends messages to each check node. The message for each bit will be either 0 or 1. There are three steps for Bit Flipping to take. Here is a thorough analysis of the algorithm for Bit flipping[19].

An example **H** Matrix shows this process step by step.

Step1<u>Initialization</u>Each bit is assigned a value.

All data is sent to the linked check nodes after this.

3, 4 and 6 check nodes are linked to the bit node 1.

The check nodes 1, 5 and 6 are joined to the bit node 2.

The check nodes 2, 3 and 5 are related to the bit node 3.

The check nodes 1, 2 and 4 are connected to bit node 4. Node Check receives bit values sent by bit nodes.

Updating Step2Parity. This time, Step2 will be repeated again and again until all the equations for parity tests are satisfied. The algorithm will terminate when all the parity check equations are satisfied, and the decoded final value will be 001011.

b) sum-product algorithm (SPA)

The sum-product algorithm is a message-passing algorithm for a soft decision. It is similar to the bit-flipping algorithm mentioned in the previous section, but now with probabilities for messages representing any decision (check met, or bit value equal to 1). The sum-product algorithm is a

soft decision algorithm that accepts the probability of each received bit as input, while bit-flipping decoding accepts an



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Published By: Blue Eyes Intelligence Engineering and Sciences Publication initial hard decision on the received bits as input. The a priori probabilities for the obtained bits are called the input bit probabilities because before running the LDPC encoder, they were known in advance[33]. a posteriori probability is referred to as the bit probabilities returned by the decoder. These probabilities are expressed as log-likelihood ratios in the case of sum-product decoding. The sum-product algorithm (SPA) asymptotically achieves the near-capacity performance The sum-product algorithm uses the soft obtained signal, which again is important when using continuous-output channels. Although the sum-product algorithm (SPAcomputational)'s complexity is very high. In practise it is difficult to implement the Sum-Product Algorithm for decoding LDPC codes, since it requires nonlinear functions and multiplications.Instead of taking the computational complexity of the SPA, to decrease $L(r_{ii})$ An approximation of that is taken, which simplifies the check node update law. The Min-Sum algorithm is known as this modified version of SPA.

c) Min-sum algorithm:

To a the complexity of the standard SPA at the cost of a noticeable degradation of decoding, a mini-sum algorithm

(MSA) has been proposed which replaces non-linear control node operation with a single minimum operation. performance. In the min-sum algorithm, the update rule for the variable node is the same as the sum-product. algorithm, but the update rule at a check node c is simplified by taking $|\mathbf{q}_{i,j}|$ term instead of $L(\mathbf{r}_{ij})$ which is actually the

approximation of the latter. The magnitude of $L(\mathbf{r}_{ij})$ computed

using min-sum approximation is usuallyTo decrease the approximation error, overestimated and correction words are added. When the magnitude of the messages is increased, this approximation becomes more precise. So in later iterations, the output of this algorithm is almost the same as that of the sum-product algorithm when the magnitude of the messages is normally high. The Min-Sum algorithm is less complicated to implement, requiring an additional signal-to-noise ratio of approximately 0.5dB to Achieving the same bit error rate as the Sum-Product algorithm by using a regular transmission LDPC code over just a binary input additive white Gaussian noise (AWGN) channel. The loss of output can be up to 1.0dB for irregular codes. approximately an additional 0.5dB of signal-to-noise ratio $\frac{E_b}{N_0}$ to achieve the same bit error rate as the Sum-Product algorithm, when using a regular LDPC code for transmission over an additive white Gaussian noise (AWGN) channel with binary input. For irregular codes, the loss in performance can be up to 1.0dB.

Table 1: Difference between Random Method and
ALgebraic Method

	-	
	ALGEBRAIC CONSTRUCTIONS	RANDOM CONSTRUCTIONS
Performance Large Block Length N≫	Perform less well	Good if the block length N is large
Performance Moderate Values of Block Length N≪	Often better	May not be sufficiently good for moderate values of N
Structure to Allow Efficient Encoding	Strong structure	Do not have a structure to allow efficient encoding
Efficient Encoding	More efficiently than random LDPC	Not efficient encoding
Complexity of Decoding	Complexity that grows only linearly with the block length.	Complexity of decoding is a lesser issue because iterative message passing algorithms allow efficient decoding
Error Floor	Low error floor	Higher error floor

XIII. CONCLUSION

This paper summaries the important concepts regarding Parity-Check Code (LDPC) for low density. It goes into the motivation of LDPC and how it is possible to decode LDPC. Different code modifications, these codes is still attractive for creating powerful codes. error correction code with reasonable complexity. As a class of concatenated codes where LDPC codes are irregular codes with different parameters interacting in parallel or in serial] with or not including interleaves, concatenated binary LDPC codes have been added. While irregular LDPC codes are more efficient than regular codes, there is an error floor and a senior level of irregular LDPC codes. encoding Complexity over regular codes . LDPC codes, based on deep and wealthy theory, are very powerful codes with huge functional possible. major advances in all core aspects of LDPC code design, review and implementation continue to be developed.

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REFERENCES

- T. T. Nguyen Ly, "Efficient Hardware Implementations Of Ldpc Decoders, Through Exploiting Impreciseness In Message-Passing Decoding Algorithms", CERG0904, 2018.
- V.Guruswamy, "Iterative Decoding of Low-Density Parity Check Codes", WA 98195, September 2006.
- W. Dan, "Improvement for LDPC Coded OFDM Communication System over Power Line", KTH, May 2013.
- 4. J. M. Jacobs, P.E. "Introduction to Error-Control Coding", by Pericles Communications Company, 2004.
- 5. B. Kurkoski, "Introduction to Low-Density Parity Check Codes.
- V.V.I Sood1,. H.P. Sinha2, A. Kalra3, "A Survey on LDPC Decoding Techniques", Vol. 1, Issue 4, ISSN No. 2249-541X, Dec 2011.
- N. S. Enad and M. H. Al-Jammal, "Performance Evaluation and Assessment of LDPC Codec over DVB-S2 and WLAN802.11n Applications", International Journal of Computer Applications (0975 – 8887) Volume 181 – No. 40, February 2019.
- X.-Y. Shih*, H.-R. Chou, "Flexible design and implementation of QC-Based LDPC decoder architecture for on-line user-defined matrix downloading and efficient decoding", Integration, the VLSI journal,2019.
- S.V., NargesR..Majid, "Combinatorial design-based quasi-cyclic LDPC codes with girth eight", journal homepage, Digital Communications and Networks 4) 296–300,2018.
- H.Gharaee, M.i Kailee and N. M. Zadeh., "A High-Throughput FPGA Implementation of Quasi-Cyclic LDPC Decoder" IJCSNS International Journal of Computer Science and Network Security, VOL.17 No.3, March 2017
- Z. Luan, Y. Pei, and N. Ge, "A fast convergence and area-efficient decoder for quasi-cyclic low-density parity-check codes," in 2013 19th Asia-Pacific Conference on Communications (APCC), 2013, pp. 458-462
- A. Abdel-Mouleh, "Non-binary LDPC codes associated to high order modulations", HAL Id:tel-01769283 https://tel.archives-ouvertes.fr/tel-01769283, Submitted on17Apr2018.
- T. B., M. Alles, T. Lehnigk-Emden, F. Kienle, N., "Low Complexity LDPC Code Decoders for Next Generation Standards", Conference Paper, DOI: 10.1145/1266366.1266437 · Source: DBLP, · January 2007.
- 14.D.-Ing. G. Lechner, "Efficient Decoding Techniques for LDPC Codes",Blumengasse 44/22, 1170 Wien geboren in Wien am 1. August 1975 Matrikelnr, July 2007.
- C.. J, S. Prathyusha, V. UshaSree, "Hard Decision and Soft Decision Decoding Algorithms of LDPC And Comparison of LDPC With Turbo Codes, RS codes And Bch Codes", Proceedings of 09th IRF International Conference, Bengaluru, India, ISBN: 978-93-84209-40-7, 27th July-2014.
- 16. A. A. YOUSSEF, "LDPC Decoding Algorithms for Implant to Implant Wireless Body Area Network", February, 2018, date of publication March 2, 2018.
- 17. Tuan Ta, "A Tutorial on Low Density Parity-Check Codes .2007.
- P. H. Siegel, "An Introduction to Low-Density Parity-Check Codes", Electrical and Computer Engineering University of California, San Diego.
- 19. S. J. Johnson, "Introducing Low-Density Parity-Check Codes".
- E.. Sonia*, E.. S. Gupta, "Hard Decision and Soft Decision Decoding Algorithms For LDPC And Qc-LDPC Codes", International Journal of Computer Science and Mobile Computing, *IJCSMC*, Vol. 4, Issue. 9, pg.182 – 191, September 2015
- M.Ezziyyani, M. Bahaj, "Advanced information technology services and system", 2017.
- 22. D.S.Patil "Design and Implementation of Unequal Error Protection Scheme for Wireless Fading Channels Using LDPC Codes for HevcBitstream". Spring 2018
- E. T. Psota, "Finite Tree-Based Decoding of Low-Density Parity-Check Codes" LLC 789, MI 48106-1346, January, 2010
- T. Richardson, "Multi-Edge Type LDPC Codes", https://www.researchgate.net/publication/37439748January 2002,
- 25. Y. Kou and S. Lin, Davis, "Low Density Parity Check Codes Based on Finite Geometries: A Rediscovery and New Results", CCR-0096191, CCR-0098029 and NASA under Grants NAG 5-9025, and NAG 5-10480.

- K.-H. Lin, R.t C. Chang, C.-L. Huang, and S.-D. Wu, "Construction of the Cyclic Block-Type LDPC Codes for Low Complexity Hardware Implementation", , 2008 IEEE.
- L.Mostari A., Abdel.Malik T.-Ahmed, "High performance short-block binary regular LDPC codes", Alexandria Engineering Journal 57, 2633–2639, (2018).
- S.B.Narang, K.Pubby, H. Kaur, "Low-density parity check (LDPC) codes: A new era incoding", SIPAIJ, 1(1), [007-014], 2016, Vol. 2, Issue 3, pp: (274-279), Month: July - September 2014.
- N. P. B havsar ,B. Vala, "Design of Hard and Soft Decision Decoding Algorithms of LDPC", International Journal of Computer Applications (0975 – 8887), Volume 90 – No 16, March 2014
- V. Chandrasetty, S. M.I Aziz, "FPGA Implementation of High Performance LDPC Decoder Using Modified 2-Bit Min-Sum Algorithm", CONFERENCE PAPER DOI: 10.1109/ICCRD.2010.186, MAY 2010.
- S. B. Narang, K.I Pubby*, H.Kaur, "Low-density parity check (LDPC) codes: Anew era in coding", SIPAIJ, 1(1), [007-014], 2016.
- M., S. A. Kumari, "Implementation Of LDPC Using Min-Sum Decoding Algorithm", ISSN 2277-2685 ,IJESR/July, / Vol-5/Issue-7/862-868, 2015.
- M.N.G. Prasadb, C.C. Reddyc, J.C. Babua, "VLSI Implementation of decoding algorithms using EG-LDPC Codes", 7th International Conference on Advances in Computing & Communications, ICACC 2017, August 22-24, Cochin, India, 2017.

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Performance Analysis of LDPC Decoding Techniques

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